Claim Amendments

Claims 20-28 have been canceled. Claims 1, 12, and 13 have been amended. Claims 2-11 and 14-19 are unchanged. The following listing of claims replaces all previous versions of the claims in the application.

Listing of Claims

1. (currently amended) Integrated circuit antifuse circuitry, comprising:

a metal-insulator-semiconductor antifuse transistor having a drain, source, gate, and substrate, wherein the drain and substrate form a drain-substrate p-n junction, wherein the substrate and source form a substrate-source p-n junction, and wherein the gate has a gate insulator; and

circuitry that applies voltages to the antifuse transistor that forward bias the substrate-source p-n junction and that cause avalanche breakdown of the drain-substrate p-n junction to produce a sufficient concentration of hot carriers to break down the gate insulator and program the antifuse transistor.

2. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the gate insulator comprises gate oxide.

3. (original) The integrated circuit antifuse circuitry defined in claim 1 further comprising sensing circuitry that senses whether the antifuse transistor has been programmed and outputs a high or low logic signal accordingly.

4. (original) The integrated circuit antifuse circuitry defined in claim 1, wherein the antifuse transistor is used on an integrated circuit having a power supply voltage, the integrated circuit antifuse circuitry further comprising a charge pump that produces a programming supply voltage having a magnitude greater than the power supply voltage, wherein the programming supply voltage is used to program the antifuse transistor.

5. (original) The integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor connected between the substrate and the source.

6. (original) The integrated circuit antifuse circuitry defined in claim 1 further comprising a conductor that electrically interconnects the gate and the source.

7. (original) The integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor that connects the drain to a positive power supply voltage.

8. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the gate is electrically connected to the source, the integrated circuit antifuse circuitry further comprising:

a first resistor connected between the drain and a positive power supply voltage; and

a second resistor connected between the substrate and a ground potential.

9. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the drain, source, and substrate are surrounded by an isolating well.

10. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages comprises at least one Zener diode connected between the drain and substrate and at least one resistor connected between the substrate and the source, wherein the Zener diode is reverse biased and breaks down to allow current

to flow from the Zener diode through the resistor to help forward bias the substrate-source p-n junction.

11. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages comprises at least one gated diode connected between the drain and substrate and at least one resistor connected between the substrate and the source, wherein the gated-diode is reverse-biased and breaks down to allow current to flow from the gated diode through the resistor to help forward bias the substrate-source p-n junction.

12. (currently amended) The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages comprises a voltage divider circuit that applies a bias voltage to the substrate during programming of the antifuse transistor to forward bias the substrate-source p-n junction.

13. (currently amended) The integrated circuit antifuse circuitry defined in claim 1 wherein the antifuse transistor is programmed during programming and is sensed during sensing and wherein the circuitry that applies the voltages comprises:

a voltage divider circuit that applies a bias voltage to the substrate during programming of the antifuse transistor to forward bias the substrate-source p-n junction; and

a switch that prevents application of the bias voltage to the substrate during sensing.

14. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the antifuse transistor is fabricated using a semiconductor fabrication process having a design rule that allows transistor gates to be fabricated with a particular minimum allowed gate length and wherein the gate of the antifuse transistor has an associated length that is greater than the minimum allowed gate length.

15. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages is formed on an integrated circuit having I/O circuitry powered by an I/O power supply voltage, wherein the circuitry that applies the voltages applies the I/O power supply voltage to the drain.

16. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the gate is electrically

connected to the source, the integrated circuit antifuse circuitry further comprising:

a resistor connected between the drain and a positive voltage; and

a second resistor connected between the substrate and a ground potential.

17. (original) The integrated circuit antifuse circuitry defined in claim 1 further comprising a current limiting resistor connected to the antifuse transistor that limits how much current is applied to the antifuse transistor when the antifuse transistor is programmed.

18. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein there are at least two different doping concentrations in the substrate adjacent to the drain so that the drain-substrate p-n junction is one of at least two parallel drain-substrate p-n junctions, wherein each of the drain-substrate p-n junctions experiences reverse breakdown at a different reverse-bias voltage level.

19. (original) The integrated circuit antifuse circuitry defined in claim 1 wherein the metal-insulator-

semiconductor antifuse transistors are formed on a silicon-on-insulator substrate.

20-28. (canceled)